REMARKS / DISCUSSION OF ISSUES

Claims 2-6, 8-12 and 26-32 are presently pending. Claims 26 and 31 are independent claims.

Rejections under 35 U.S.C. § 102

Claims 2-6, 8-12 and 26-32 were rejected under 35 U.S.C. § 102(b) in view of *Lepejian, et al.* For at least the reasons set forth herein, it is respectfully submitted that the pending claims are patentable over the applied art.

A proper rejection for anticipation requires, as the first step in the inquiry, that all the elements of the claimed invention be described in a single reference. A necessary corollary to the test of anticipation is that the absence from the reference of any claimed element negates anticipation.

Initially, the rejection of claim 30 under 35 U.S.C. § 102 is wholly improper. In particular, at page 9 of the Office Action dated August 8, 2005, the Examiner notes that the reference to *Lepejian, et al.* lacks the disclosure of the decoder's being a lookup table implemented in read only memory. Accordingly, because the applied reference lacks at least one feature of claim 30, it cannot serve to establish a *prima facie* case of anticipation. Withdrawal of this rejection is earnestly solicited.

Claim 26 features:

*"...a memory element in an integrated circuit, the **memory element having** at least one deterministic operation and **at least one non-deterministic operation** controllable by at least two control lines..."*

Claim 31 features:

*"...providing an integrated circuit having a memory element, **the memory element having** at least one deterministic operation **and at least one non-deterministic operation** controllable by at least two control lines..."*

It is respectfully submitted that the reference to *Lepejian, et al.* lacks at least the disclosure of the noted features of claims 26 and 31. The filed

application defines non-deterministic operations to be "contention conditions that would not occur during actual operation of the IC". For example, a non-deterministic operation is a stimulus that attempts to read and write to the same location in a memory. As noted in the filed application, a built in self-test (BIST) result that included such a simultaneous read-write operation is also non-deterministic and renders the test unusable for its intended purpose. It is stimulation of the nondeterministic operations during a built in self-test ("BIST") **that is avoided** in the method of claim 26 and the apparatus of claim 31. (See page 2, lines 5-16 and page 6, lines 15-26 of the present Specification.

The Office Action asserts that the reference to *Lepejian, et al.* discloses "testing transition and capacitive coupled faults, which corresponds to a non-deterministic operation." The Examiner notes that the transition and capacitive coupling faults are random unpredictable faults that are not detected and that appear only at normal speed operation. (See pages 2 and 3 of the August 8, 2005 Office Action.)

In describing a method of reducing area on a chip (IC) devoted to data buses, the reference to *Lepejian, et al.* describes the use of a serial data-in line and a data-out line. The reference notes that this method is disadvantageous because the memory is tested at much less than operational frequency. The transition and capacitive coupling faults described in *Lepejian, et al.* are actual faults inherent in the tested product that are found by testing deterministic operations at full speed and detecting a test failure. Thus, these faults that appear only during the **normal** operational frequencies are not detected during the disclosed testing procedure. (See col. 2, lines 15-29 and col. 3, lines 53-58 of the reference to *Lepejian, et al.*).

Clearly, the referenced faults **do occur** during normal operation of the IC. Therefore by the definition provided in the filed application these faults cannot be non-deterministic operations that **would not occur** during actual operation of the IC. Moreover, as noted above, the Examiner states that the transition and capacitive coupling faults are **not detected** and that normally **appear at normal speed operation**. However, per the definition provided in the filed application, a

non-deterministic operation would not occur during actual operation of the IC, let alone be detected in a test. Stated differently, the transition and capacitive coupling faults do occur during actual operation of the IC, regardless of their detection in a test. Therefore, these faults are not non-deterministic operations as recited in the independent claims.

For at least the reasons set forth above, it is respectfully submitted that the reference to *Lepejian, et al.* lacks at least the disclosure of one feature of each of claims 26 and 31. Because the reference to *Lepejian, et al.* lacks the disclosure of at least one of the features of claims 26 and 31, it cannot serve to establish a *prima facie* case of anticipation thereof. Therefore, claims 26 and 31 and the claims that depend therefrom are patentable over the applied art. Allowance is solicited.

Rejections under 35 U.S.C. § 103

Claims 30 was rejected under 35 U.S.C. § 102(b) in view of *Lepejian, et al.* further in view of *Powell, et al.*

While in no way conceding to the propriety of the rejection, Applicants respectfully submit that claim 30 is allowable over the applied art at least because of its dependence on claim 26, which is allowable for at least the reasons set forth above.

The above notwithstanding, Applicants respectfully traverse the propriety of the combination of *Lepejian, et al.* and *Powell, et al.* It is well-established that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a reason, suggestion or motivation do so. The reason, suggestion or motivation may come from references themselves; from knowledge of those skilled in art that certain references or disclosures in references are known to be of interest in the particular field; or from nature of the problem to be solved to do so found in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

The motivation to combine references garners no support from the

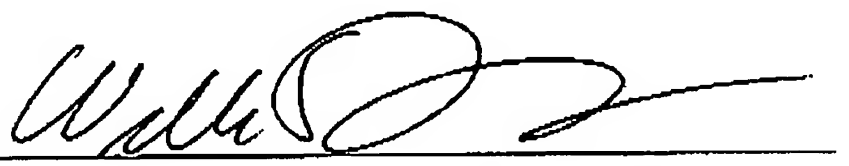
references themselves. If the motivation is from knowledge of those skilled in the art or references of interest, Applicants respectfully request that these references or other suitable extrinsic evidence be provided. If the motivation is from the personal knowledge of the Examiner, an affidavit under 37 CFR § 1.104(d)(2) is respectfully requested. If evidence in support of the assertions of inherency are not provided it is respectfully submitted that the rejections based on inherency be withdrawn.

Conclusion

In view of the foregoing, Applicant respectfully requests that the objections and rejections of record be withdrawn, and all pending claims be allowed. If any remaining issues can be resolved through a personal or telephonic interview, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted on behalf of:

Agilent Technologies, Inc.



by: William S. Francos (Reg. No. 38,456)

Date: October 11, 2005

Volentine, Francos & Whitt, PLLC
Treeview Corporate Center
Two Meridian Blvd.
Wyomissing, PA 19610
(610) 375-3513 (v)
(610) 375-3277 (f)